UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

JAMES B. GOODMAN,

Plaintiff

v.

HPE, INC.,

Defendant

Case No. 6:20-cv-702

JURY TRIAL DEMANDED

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff James B. Goodman ("Plaintiff" or "Goodman") hereby files this Original Complaint for Patent Infringement against Defendant HPE, Inc. ("Defendant" or "HPE"), and alleges, on information and belief, as follows:

THE PARTIES

1. James B. Goodman is an individual residing in Texas.

2. On information and belief, Defendant HPE, Inc. is a company organized and existing under the laws of Texas, with a principal place of business at 5100 Cape Ann Drive, Corpus Christi, Texas 78412. HPE, Inc. may be served through its registered agent, Henry P. Ellsworth, at 5100 Cape Ann Drive, Corpus Christi, Texas 78412.

JURISDICTION AND VENUE

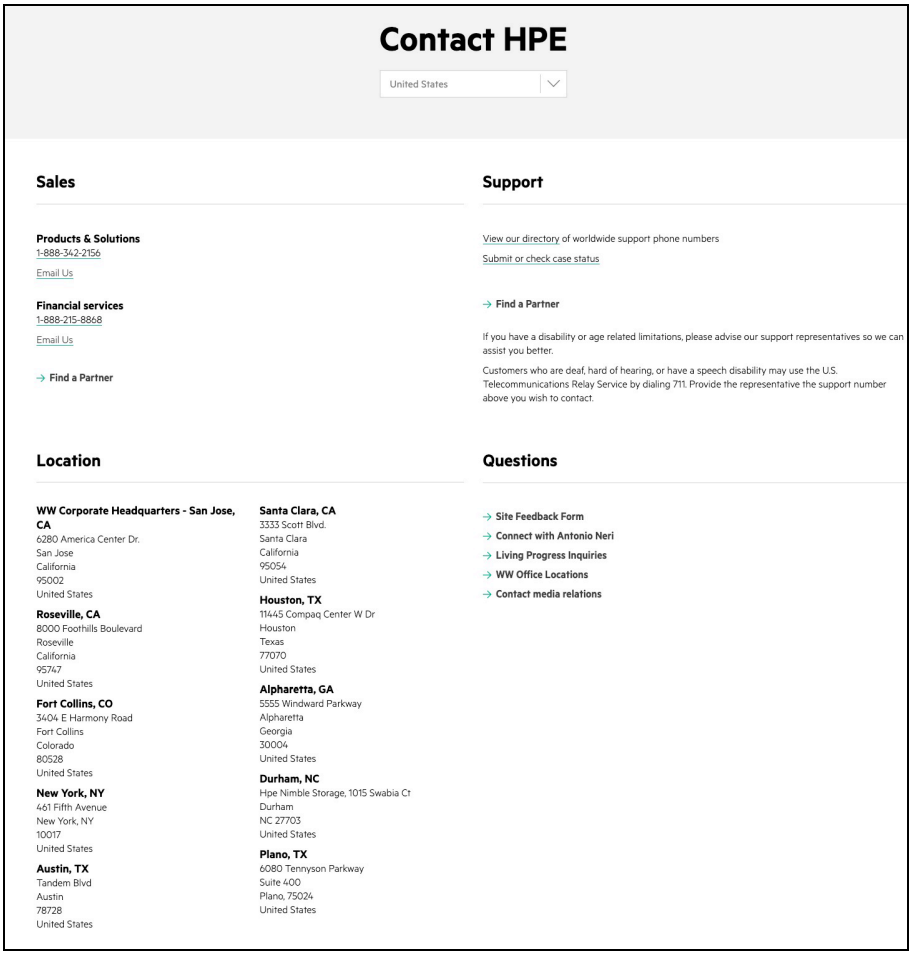
3. This action arises under the patent laws of the United States, 35 U.S.C. § 1, *et seq*. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331, 1332 and 1338(a).

4. Defendant has committed acts of infringement in this judicial district.

5. On information and belief, Defendant maintains regular and systematic business interests in this district and throughout the State of Texas including through its representatives, employees and physical facilities.

6. On information and belief, the Court has personal jurisdiction over Defendant because Defendant has committed, and continues to commit, acts of infringement in the State of Texas, has conducted business in the State of Texas, and/or has engaged in continuous and systematic activities in the State of Texas. On information and belief, Defendant's accused instrumentalities that are alleged herein to infringe were and continue to be used, imported, offered for sale, and/or sold in the Western District of Texas.

7. On information and belief, Defendant voluntarily conducts business and has job openings currently in the State of Texas and within this District, including, but not limited to, its offices located at Tandem Blvd., Austin, Texas 78728. *See, e.g.:*



Contact HPE

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Customers who are deaf, hard of hearing, or have a speech disability may use the U.S. Telecommunications Relay Service by dialing 711. Provide the representative the support number above you wish to contact.

Location

WW Corporate Headquarters - San Jose, CA
6280 America Center Dr.
San Jose
California
95002
United States

Roseville, CA
8000 Foothills Boulevard
Roseville
California
95747
United States

Fort Collins, CO
3404 E Harmony Road
Fort Collins
Colorado
80528
United States

New York, NY
461 Fifth Avenue
New York, NY
10017
United States

Austin, TX
Tandem Blvd
Austin
78728
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77070
United States

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5555 Windward Parkway
Alpharetta
Georgia
30004
United States

Durham, NC
Hpe Nimble Storage, 1015 Swabia Ct
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NC 27703
United States

Plano, TX
6080 Tennyson Parkway
Suite 400
Plano, 75024
United States

Questions

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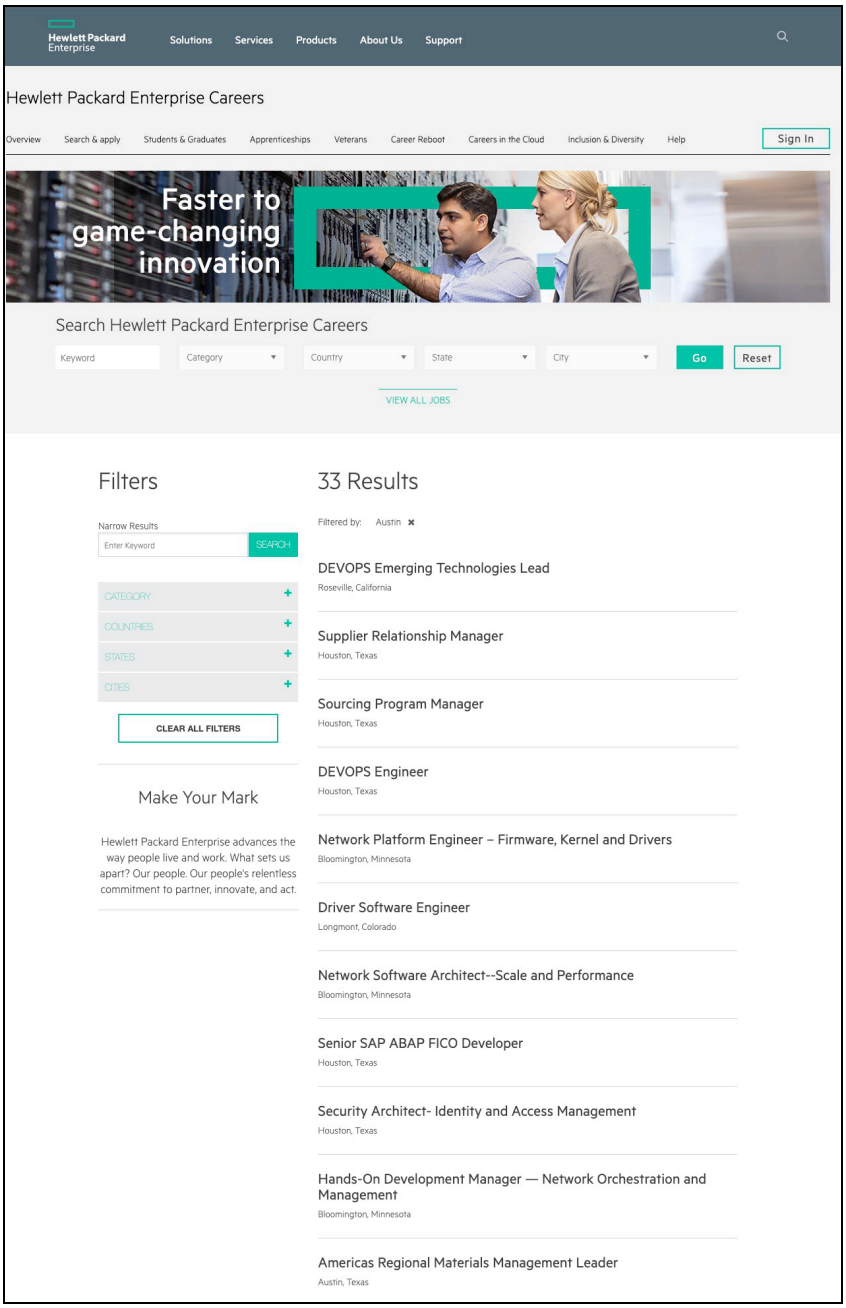
HPE website as visited on July 28, 2020: https://www.hpe.com/us/en/contact-hpe.html#location.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Make Your Mark
Hewlett Packard Enterprise advances the way people live and work. What sets us apart? Our people. Our people's relentless commitment to partner, innovate, and act.
33 Results
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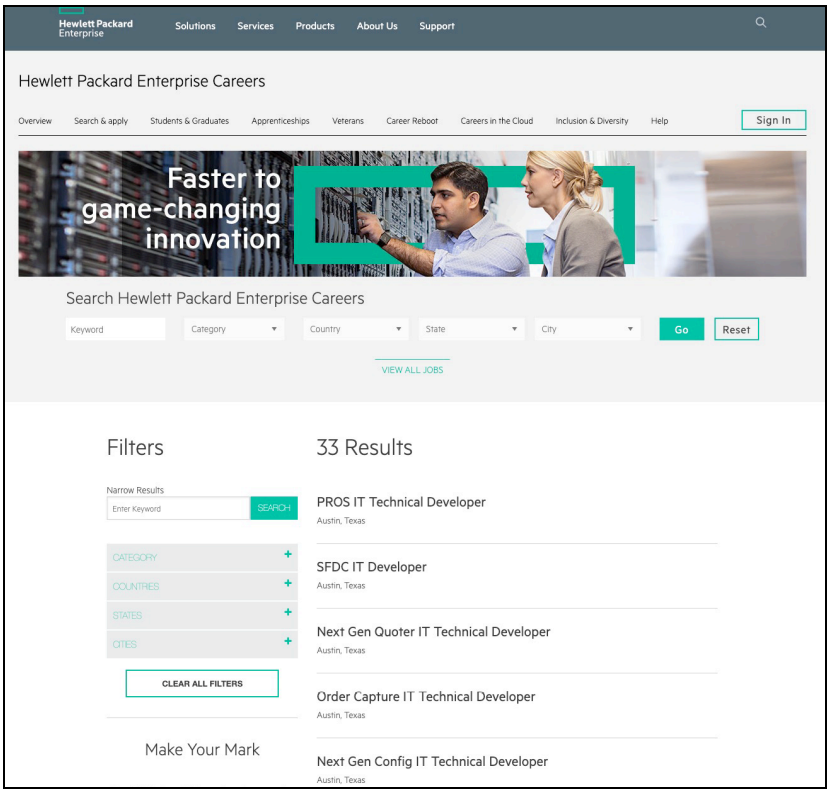
Houston, Texas
Security Architect- Identity and Access Management
Houston, Texas
Hands-On Development Manager — Network Orchestration and Management
Bloomington, Minnesota
Americas Regional Materials Management Leader
Austin, Texas



HPE website as visited on July 28, 2020 at: https://careers.hpe.com/jobs.

8. On information and belief, Defendant generates substantial revenue within this District and from the acts of infringement as carried out in this District. As such, the exercise of jurisdiction over Defendant would not offend the traditional notions of fair play and substantial justice.

9. Venue is proper in the Western District of Texas pursuant to 28 U.S.C. § 1400(b) and 28 U.S.C. § 1391(c)(3).

NOTICE OF GOODMAN'S PATENTS

10. Goodman is the inventor and owner of U.S. Patent No. 4,617,624B2 ("the '624 Patent") entitled "Multiple configuration memory circuit." A copy may be obtained at: https://patents.google.com/patent/US4617624A/

11. Goodman is the inventor and owner of U.S. Patent No. 6,243,315B1 ("the '315 Patent" and "the Patent-in-Suit") entitled "Computer memory system with a low power down mode." A copy may be obtained at: https://patents.google.com/patent/US6243315B1/ .

12. Goodman is the co-inventor and co-owner of U.S. Patent No. 6,257,911B1 ("the '911 Patent") entitled "Low insertion force connector with wipe." A copy may be obtained at: https://patents.google.com/patent/US6257911.

13. The foregoing Patents are collectively referred to as "the Goodman Patents."

14. The Goodman Patents are valid, enforceable, and were duly issued in full compliance with Title 35 of the United States Code.

15. Defendants, at least by the date of this Original Complaint, are on notice of the Goodman Patents.

ACCUSED INSTRUMENTALITIES

16. On information and belief, Defendants make, use, import, sell, and/or offer for sale a multitude of products and services as memory systems relying on HPE DDR4 SmartMemory and the JESD79-4B standard including, but not limited to:

- HPE ProLiant DL380 Gen10 Server;
- HPE 8GB (1x8GB) Single Rank x8 DDR4-2933 CAS-21-21-21 Registered Smart Memory Kit P00918-B21;
- HPE 8GB (1x8GB) Single Rank x8 DDR4-2666 CAS-19-19-19 Registered Smart Memory Kit 815097-B21;
- HPE 16GB (1x16GB) Single Rank x4 DDR4-2933 CAS-21-21-21 Registered Smart Memory Kit P00920-B21;
- HPE 16GB (1x16GB) Single Rank x4 DDR4-2666 CAS-19-19-19 Registered Smart Memory Kit 815098-B21;
- HPE 16GB (1x16GB) Dual Rank x8 DDR4-2933 CAS-21-21-21 Registered Smart Memory Kit P00922-B21;
- HPE 16GB (1x16GB) Dual Rank x8 DDR4-2666 CAS-19-19-19 Registered Smart Memory Kit 835955-B21;
- HPE 32GB (1x32GB) Dual Rank x4 DDR4-2933 CAS-21-21-21 Registered Smart Memory Kit P00924-B21;

- HPE 32GB (1x32GB) Dual Rank x4 DDR4-2666 CAS-19-19-19 Registered Smart Memory Kit 815100-B21;
- HPE 64GB (1x64GB) Dual Rank x4 DDR4-2933 CAS-21-21-21 Registered Smart Memory Kit P00930-B21 Load Reduced DIMMs (LRDIMMs);
- HPE 64GB (1x64GB) Quad Rank x4 DDR4-2933 CAS-21-21-21 Load Reduced Smart Memory Kit P00926-B21;
- HPE 64GB (1x64GB) Quad Rank x4 DDR4-2666 CAS-19-19-19 Load Reduced Smart Memory Kit 815101-B21;
- HPE 128GB (1x128GB) Octal Rank x4 DDR4-2933 CAS-24-21-21 Load Reduced 3DS Smart Memory Kit P00928-B21;
- HPE 128GB (1x128GB) Octal Rank x4 DDR4-2666 CAS-22-19-19 3DS Load Reduced Memory Kit 815102-B21 (individually and collectively, the "Accused Instrumentalities").

17. On information and belief, the Accused Instrumentalities are made, used, sold, offered for sale, and/or imported in the United States by Defendants.

COUNT I
(Infringement of U.S. Patent No. 6,243,315B1)

18. Goodman incorporates the above paragraphs by reference.

19. Defendant has been on notice of the '315 Patent at least as early as the date it received service of this Original Complaint.

20. On information and belief, Defendant has directly infringed and continue to infringe the '315 Patent by making, using, importing, selling, and/or, offering for sale the Accused Instrumentalities in the United States.

21. On information and belief, Defendant, with knowledge of the '315 Patent, indirectly infringes the '315 Patent by inducing others to infringe the '315 Patent. In particular, Defendant intends to induce customers to infringe the '315 Patent by encouraging customers to use the Accused Instrumentalities in a manner that results in infringement.

22. On information and belief, Defendant also induces others, including its customers, to infringe the ’315 Patent by providing technical support for the use of the Accused Instrumentalities.

23. On information and belief, the Accused Instrumentalities necessarily infringe one or more claims of the ‘315 Patent when used as intended.

24. On information and belief, the Accused Instrumentalities infringe at least Claim 5 of the ’315 Patent by providing a memory system for use in a computer system that have a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and capable of being placed in a self refresh mode. For example, the memory systems are DRAM semiconductor microchips. Further, Defendant provides a memory system that is compatible with the dimensions and pin assignments in accordance with JEDEC industry standard 144 PIN SODIMM connector. Further, Defendant provides a control device for selectively electrically isolating memory devices from respective address lines and respective control lines so that when the memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices as meaning that the control device electrically isolates the memory devices from all address and control lines that communicate with the memory devices. , *See e.g.,*

Claim 1. A memory system for use in a computer system, said memory system comprising: a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and	The Smart Modular Court has determined that a "memory system" is "**a system capable of retaining data**". The JESD Standard No. 79-4B, P 9 Section 3.2 Basic Functionality states the DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bank group for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins. The Smart Modular Court has determined that "memory device" means "**integrated circuit or chip**"; that "a plurality of volatile solid state memory devices" means "**two or more memory devices in the memory system into which data may be written or from which data may be retrieved that retain information while a electrical power source, having a predetermined voltage range, is applied to the memory devices and when the voltage reaches a predetermined threshold outside of that range, the memory devices will no longer retain their current state of information**" The JESD79-4B at p. 123 refers to the DDR4 SDRAM as being a "chip". See Sec. 4.26 stating, "the chip enters a Refresh cycle". It appears that the DDR4 is a chip. The JESD79-4B at sec. 3.2 p. 9 refers to the DDR4 SDRAM as being at the "**internal DRAM core**". It appears that the DDR4 **internal DRAM core** is an **integrated circuit**.

	The JESD79-4B at p. 150, Table 62 states the absolute maximum DC Ratings. P. 151, Table 63 shows the recommended DC Operating Conditions with a minimum and maximum for the DC voltages. It appears that the DDR4 requires a specific range of applied of voltage to retain data.
capable of being placed in a self refresh mode;	The JESD79-4B identifies the DDR4 as having a memory array in the description of A0-A15. See also p. 5, Sec. 4.30.4, "... no refresh activities in the memory arrays ..." The JESD79-4B shows that the DDR4 is capable of being refreshed at the following places: p. 37, Sec. 4.9.5 entitled, "Self Refresh entry and exit"; p. 123, Sec. 4.26 entitled, "Refresh Command"; and p. 124, Sec. 4.27 entitled, "Self refresh Operation". JESD79-4B, Page 5 2.6 Input Description shows CKE HIGH activates, and CKE Low **deactivates**, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh. NOTE 15 "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins. JESD79-4B, P 124 The Self-Refresh command can be used to retain data in the DDR4 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR4 SDRAM retains

	data without external clocking. The DDR4 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS_n, RAS_n/A16, CAS_n/A15, and CKE held low with WE_n/A14 and ACT_n high at the rising edge of the clock. Before issuing the Self-Refresh-Entry command, the DDR4 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD,tRFC, tZQinit, tZQoper, tZQCS, etc.). Deselect command must be registered on last positive clock edge before issuing Self Refresh Entry command. JESD79-4B, P124, When the DDR4 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET_n, are "don't care. JESD79-4B, P5, CKE HIGH activates, and CKE Low **deactivates**, internal clock signals and **device input buffers** and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
said memory devices having address lines and control lines; a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and	The Court has determined that "control device" means "**a device in the memory system that is interposed between the respective address lines and respective control lines that electrically isolates the memory devices**"; that "selectively electrically isolating said memory devices from respective address lines and respective control lines' means "**inhibiting signals on the respective address and respective control lines from the memory devices such that signals on those lines do not arrive at the memory devices**"; that "address

	lines" mean "**lines that carry signals specifying a memory location to be accessed**"; "control lines" mean "**lines that carry control signals**"; and "control signals" mean "**signals that control the sequence of addressing and the memory mode**". During testing and evaluation of the DDR4, it is necessary for Smart Modular to connect subsystems to the DDR4 using the input and output terminals of the DDR4. Obviously, the use of the term "interposed" relates to the electrically operation of the control device, not a physical positioning. The JESD79-4B at p. 5, Sec. 2.6 identifies **address lines** connected to inputs such as for symbols "BA0-BA2", and "A0-A15". The JESD79-4B uses the terms "command signal", and "command line" for the defined "**control signal**" and "control line". At p. 13, Sec. 2.3, RAS, CAS, WE (line over each) are command inputs. The command signals on the input terminals connect into the DDR4 on "control lines" to control the sequence and memory mode. See p. 24, Sec. 4.1
a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.	JESD79-4B, p. 124, Sec. 4.27 states, the Self-Refresh command can be used to retain data in the DDR4 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR4 SDRAM retains data without external clocking.The DDR4 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS_n, RAS_n/A16, CAS_n/A15, and CKE held low with WE_n/A14 and ACT_n high at the rising edge of the clock. Before issuing the Self-Refresh-Entry command, the DDR4 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD,tRFC, tZQinit, tZQoper, tZQCS, etc.). Deselect command must be registered on last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh

	Entry command is registered, Deselect command must also be registered at the next positive clock edge. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the DDR4 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET_n, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VPP, and VRefCA) must be at valid levels. JESD79-4B, Page 25 Sec. 4.2 CKE Truth Table **Table 17** NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state. JESD79-4B, Page 25 Sec. 4.2 CKE Truth Table **Table 17** NOTE 13 Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See 4.27 "Self-Refresh Operation" on page 124 and See 4.28 "Power-Down Modes" on page 127. Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. JESD 79-4B Sec.4.26 Refresh Command The Refresh command (REF) is used during normal operation of the DDR4 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR4 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When CS_n, RAS_n/A16 and CAS_n/A15 are held Low and WE_n/A14 and ACT_n are held High at the rising edge of the clock, **the chip enters a Refresh cycle**. JESD79-4B, P. 9 Sec. 3.2 Basic Functionality states the DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank
5. The memory system as claimed in claim 1, wherein the memory devices are DRAM semiconductor microchips.	

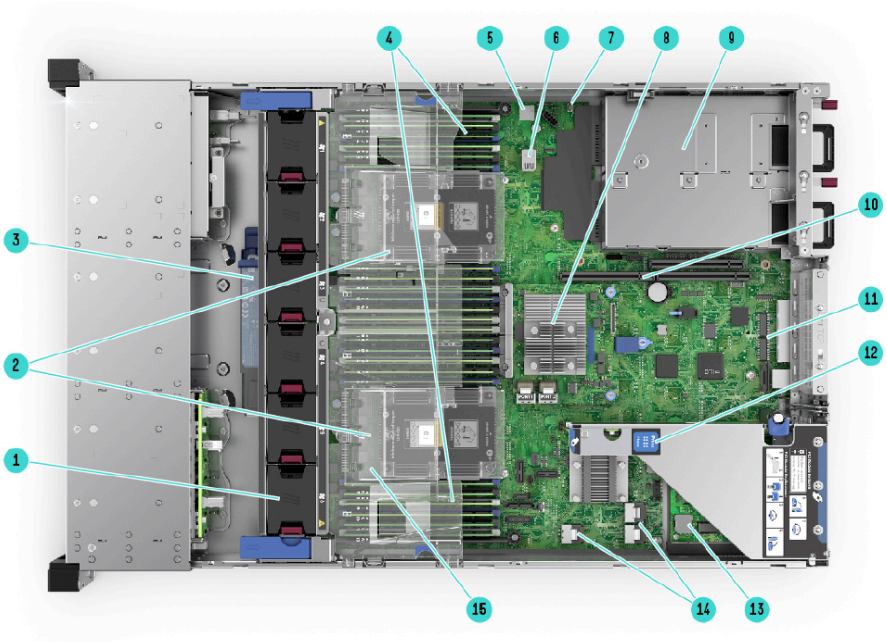
	group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins. JESD79-4B P2, Section 2 DDR4 SDRAM Package Pinout and Addressing.

2.7 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c. ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Set commands.A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.

JESD79-4B Standard Website as visited on July 28, 2020:
http://www.softnology.biz/pdf/JESD79-4B.pdf.

Overview



Internal View 8SFF chassis – with optional 2nd CPU, FlexLOM, Smart array shown

1. Fan cage shown with 6 standard Hot-plug fans (High Performance temperature fans optional)
2. 2 Processors, heatsink showing
3. Optional HPE Smart Hybrid Capacitor or HPE Smart Storage Battery
4. DDR4 DIMM slots. Shown fully populated in 24 slots (12 per processor)
5. MicroSD card slot (Optional Dual Micro-SD option)
6. Internal USB 3.0 connector
7. Chassis intrusion detection connector
8. Optional HPE Smart Array (P408i-a shown)Clear air baffle
9. (Under) Hot Plug redundant HPE Flexible Slot Power supplies
10. Connection for second (optional) riser (Requires second CPU)
11. Embedded 4x1Gbe NIC
12. Primary PCIe riser, standard (Optional double wide GPU riser)
13. Optional Flexible LOM slot
14. X4 SATA ports (1, 2 and 3)
15. Clear air baffle

QuickSpecs HPE ProLiant DL380 Gen10 Server Overview, p. 3.

PRAYER FOR RELIEF

WHEREFORE, Goodman respectfully requests the Court enter judgment against Defendant:

1. declaring that the Defendant has infringed each of the Patent-in-Suit;

2. awarding Goodman its damages suffered as a result of Defendant's infringement of the Patent-in-Suit;

3. awarding Goodman its costs, attorneys' fees, expenses, and interest;

4. awarding Goodman ongoing post-trial royalties; and

5. granting Goodman such further relief as the Court finds appropriate.

JURY DEMAND

Goodman demands trial by jury, under Fed. R. Civ. P. 38.

Dated: July 30, 2020

Respectfully Submitted

/s/ M. Scott Fuller

M. Scott Fuller
Texas Bar No. 24036607
sfuller@ghiplaw.com
Thomas G. Fasone III
Texas Bar No. 00785382
tfasone@ghiplaw.com
GARTEISER HONEA, PLLC
119 W. Ferguson Street
Tyler, Texas 75702
Telephone: (903) 705-7420
Facsimile: (888) 908-4400

ATTORNEYS FOR PLAINTIFF
JAMES B. GOODMAN